

APR 30 2004

Atty. Dkt. No. 045054-0158

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Hitoshi IRINO  
Title: SEMICONDUCTOR PROTECTION ELEMENT, SEMICONDUCTOR  
DEVICE AND METHOD FOR MANUFACTURING SAME  
Appl. No.: 10/796,999  
Filing Date: 03/11/2004  
Examiner: Unassigned  
Art Unit: Unassigned

**TRANSMITTAL OF FORMAL DRAWINGS**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

ATTENTION: DRAWING REVIEW BRANCH

Sir:

Transmitted herewith are the formal drawings (16 sheets, Figures 1-2, 3A-3B, 4A-4B, 5-28, 29A-29B) for the above-identified application. The Official Draftsperson is respectfully requested to approve these drawings for entry into the application.

Respectfully submitted,

Date: April 30, 2004

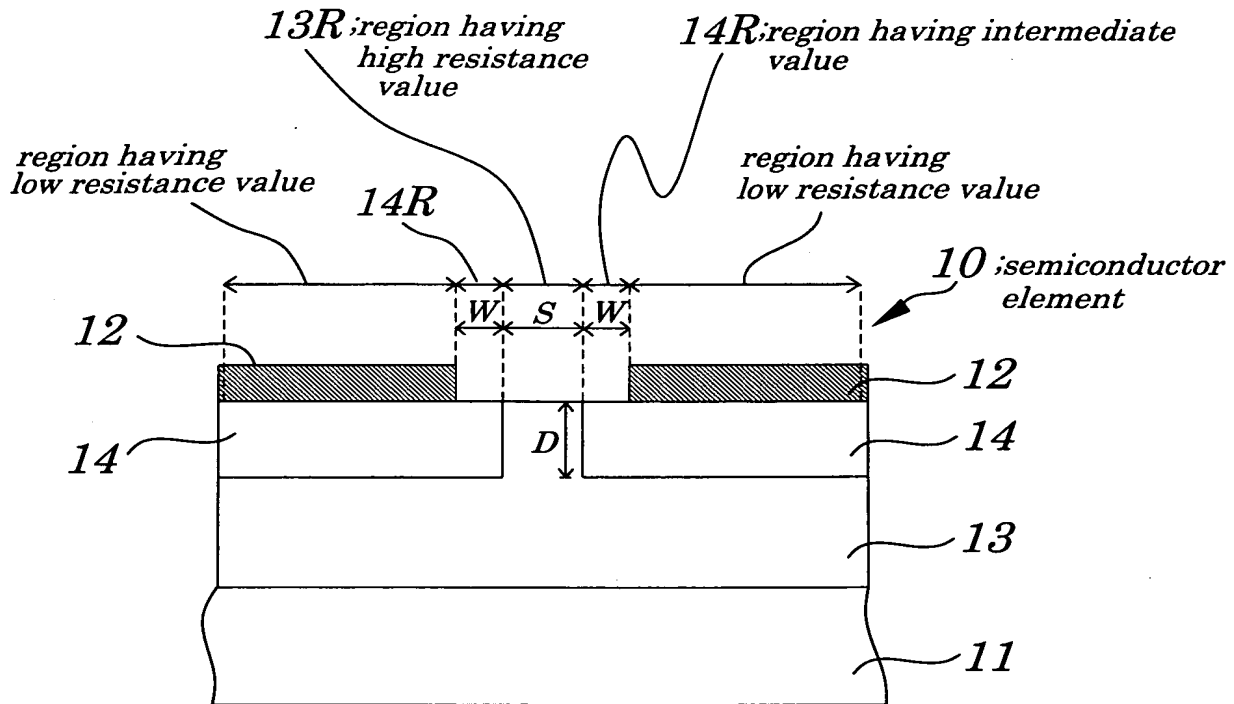
FOLEY & LARDNER LLP  
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By Thomas J. Bebban Reg. No. 43438

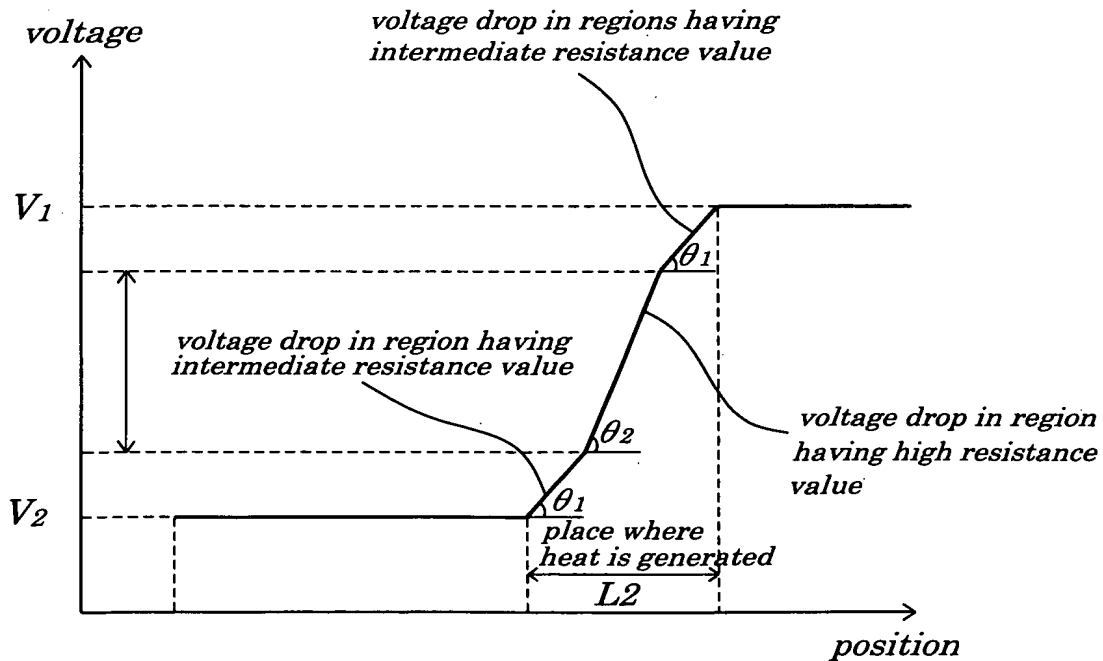
for David A. Blumenthal  
Attorney for Applicant  
Registration No. 26,257



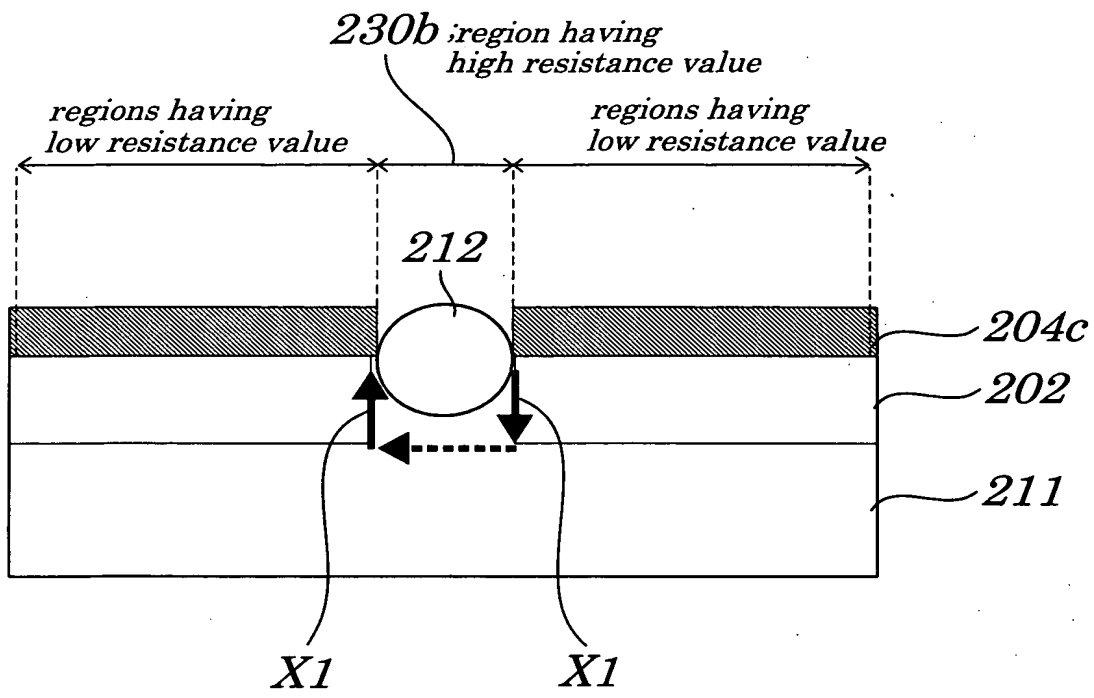
**FIG.1**



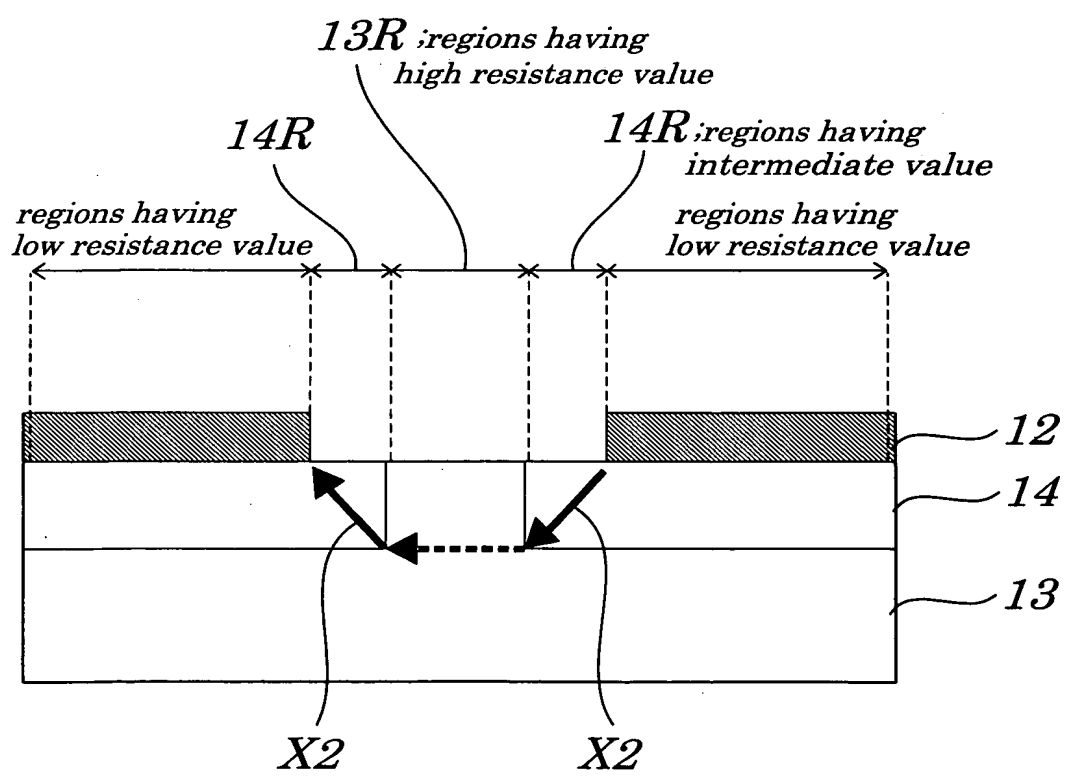
**FIG.2**



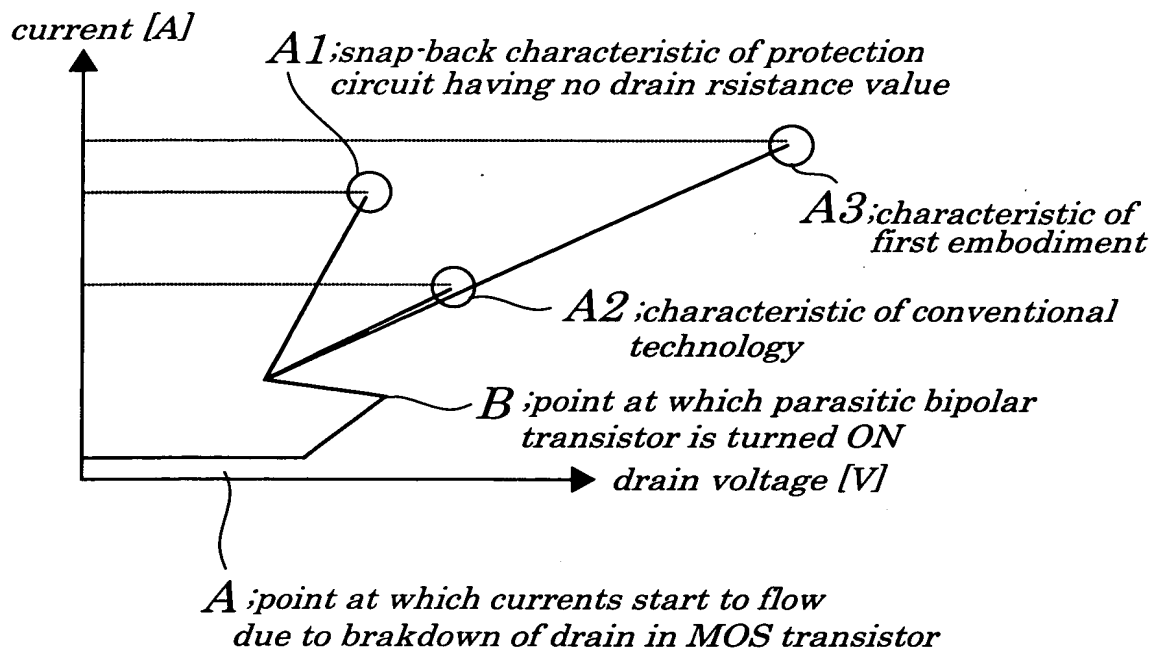
**FIG. 3A (PRIOR ART)**



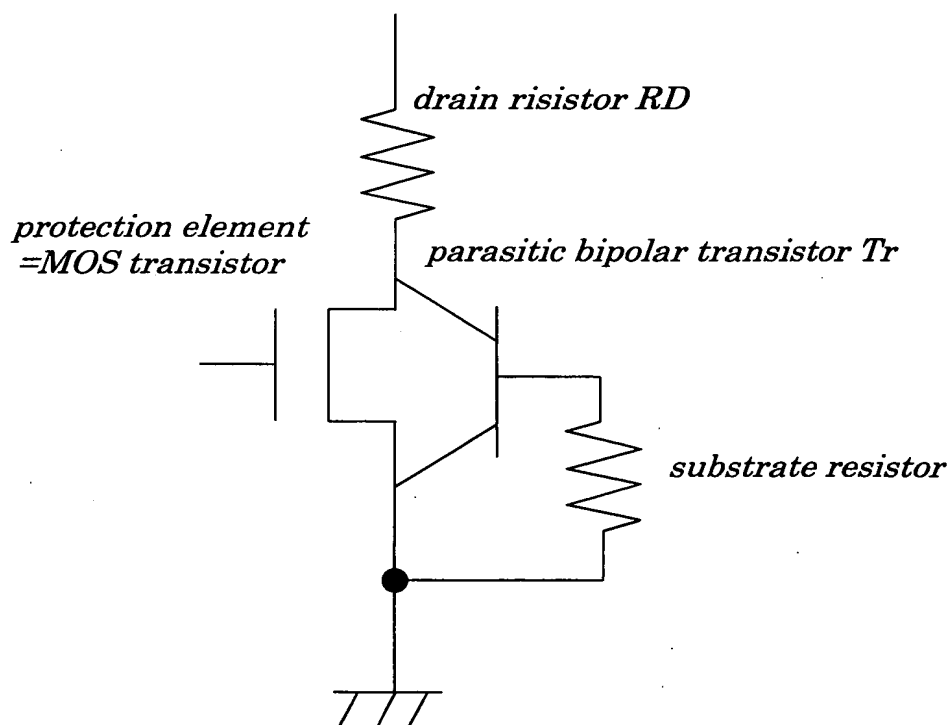
**FIG. 3B**



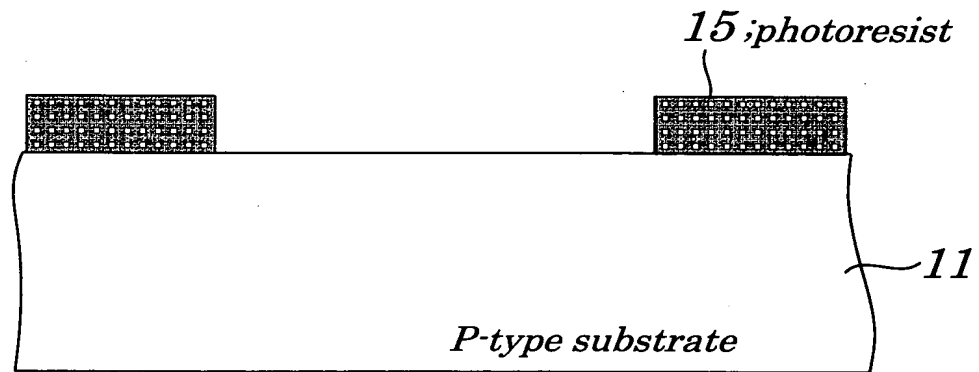
**FIG. 4A**



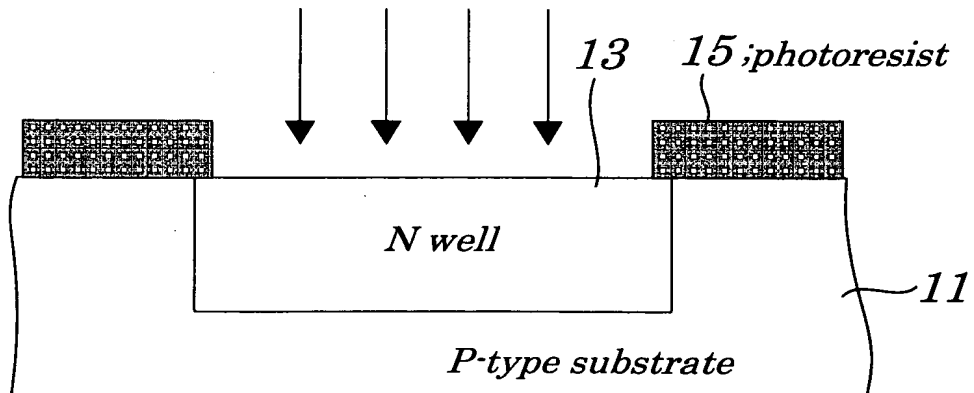
**FIG. 4B**



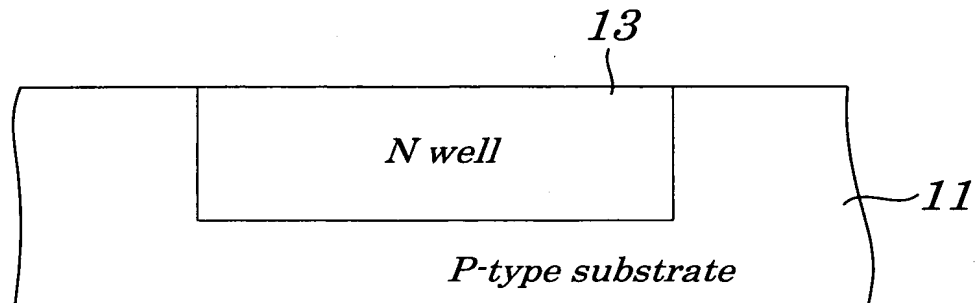
**FIG. 5**



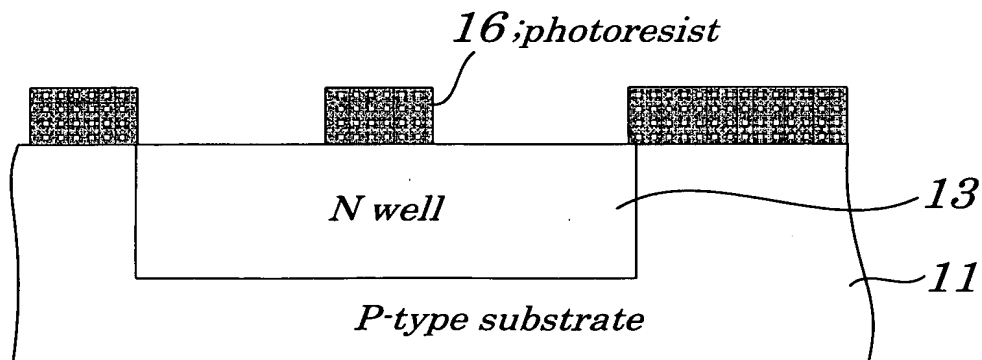
**FIG. 6**



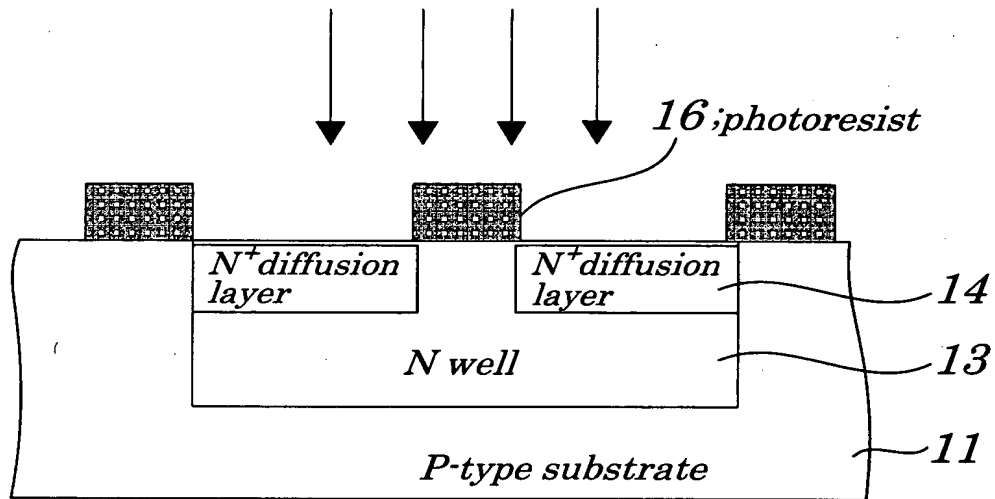
**FIG. 7**



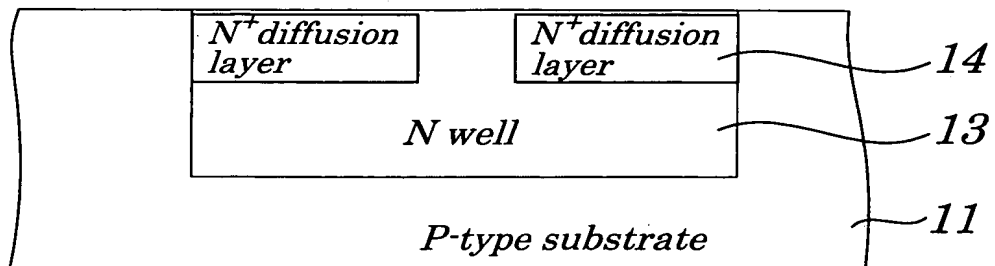
**FIG. 8**



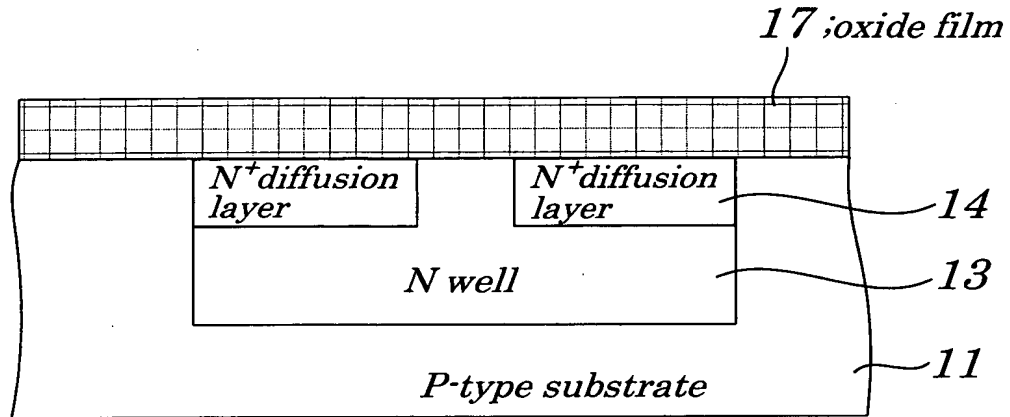
**FIG.9**



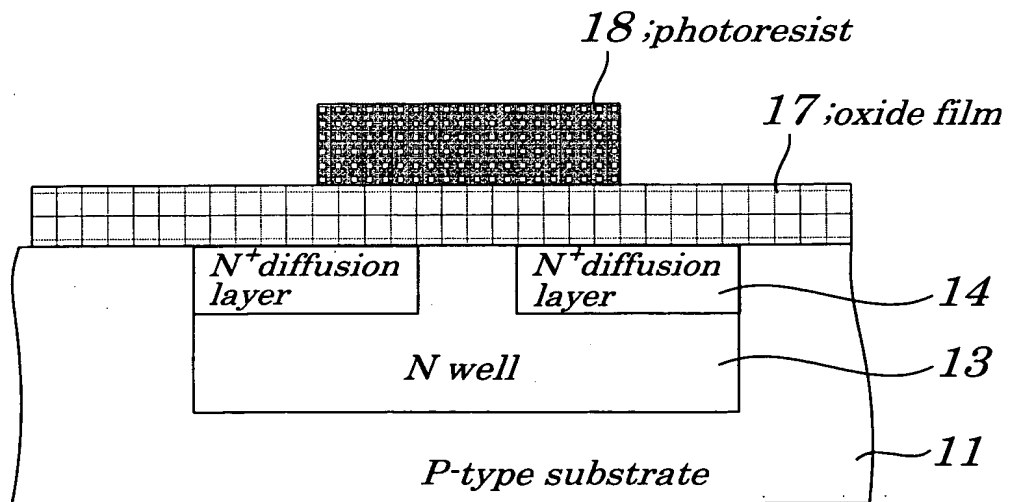
**FIG.10**



**FIG. 11**

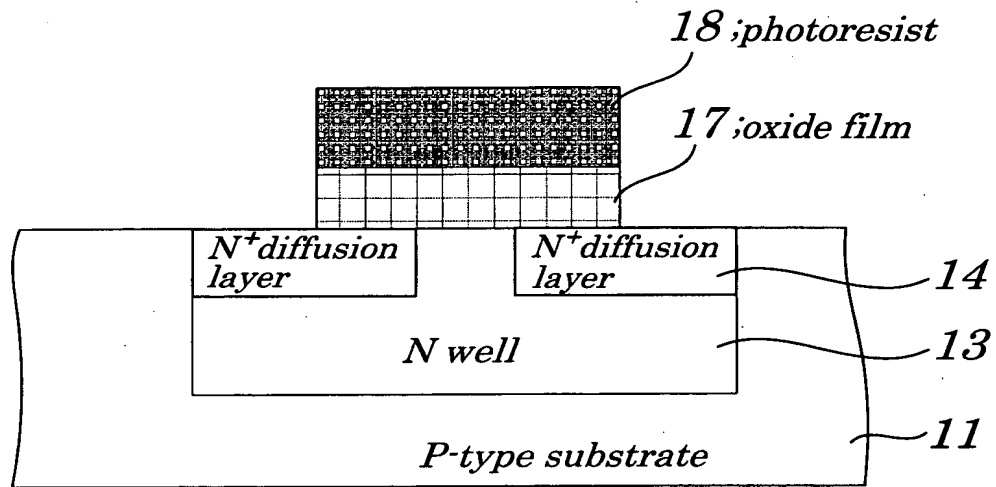


**FIG. 12**

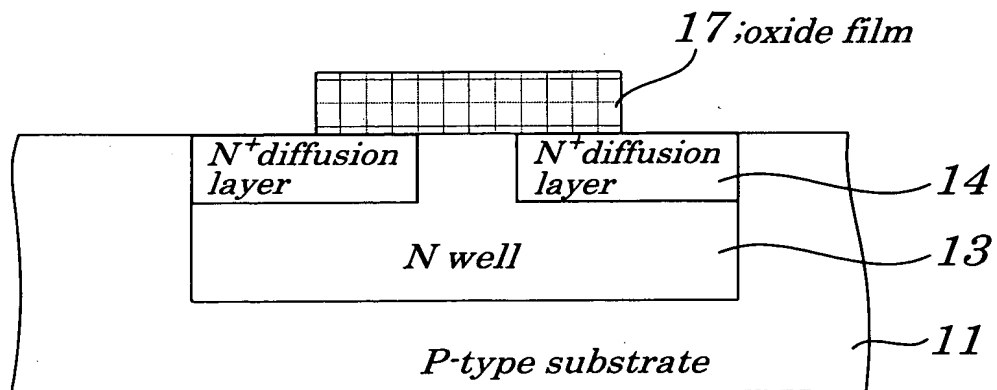




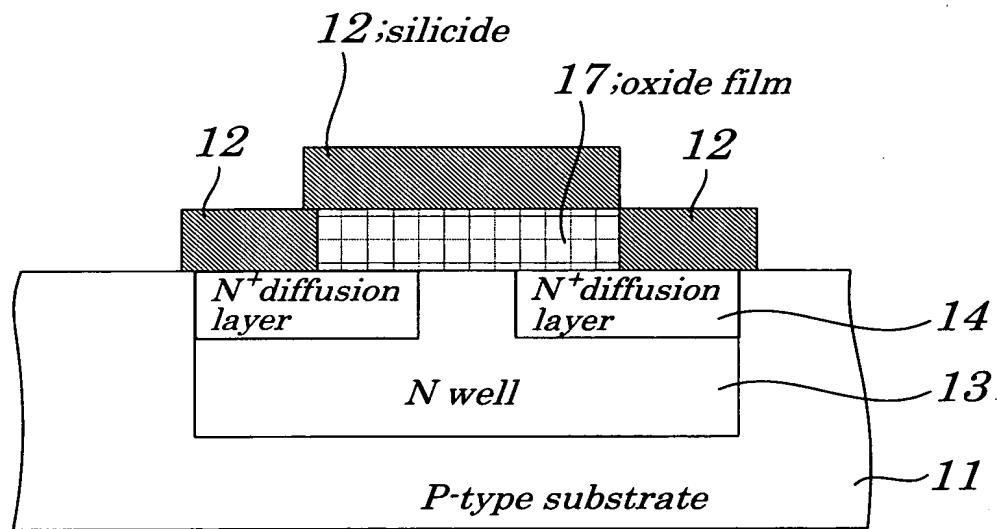
**FIG.13**



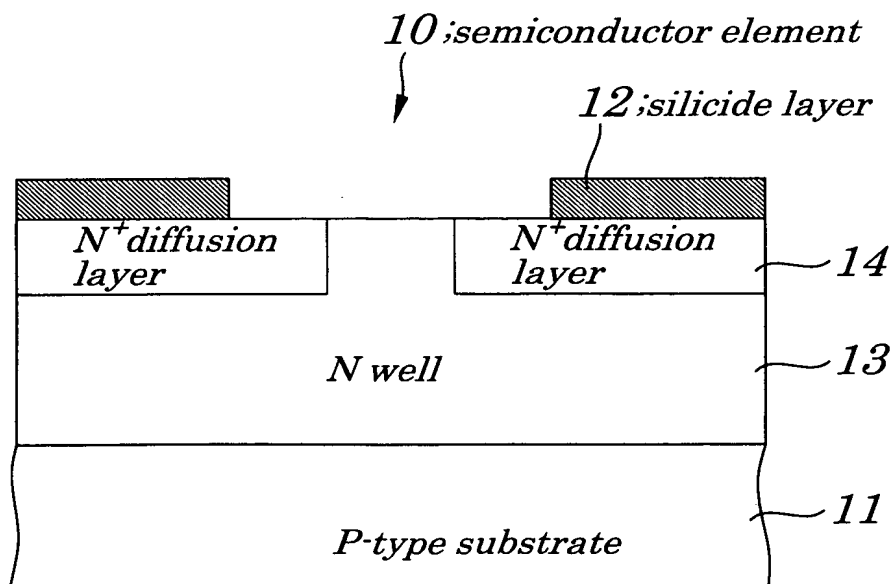
**FIG.14**



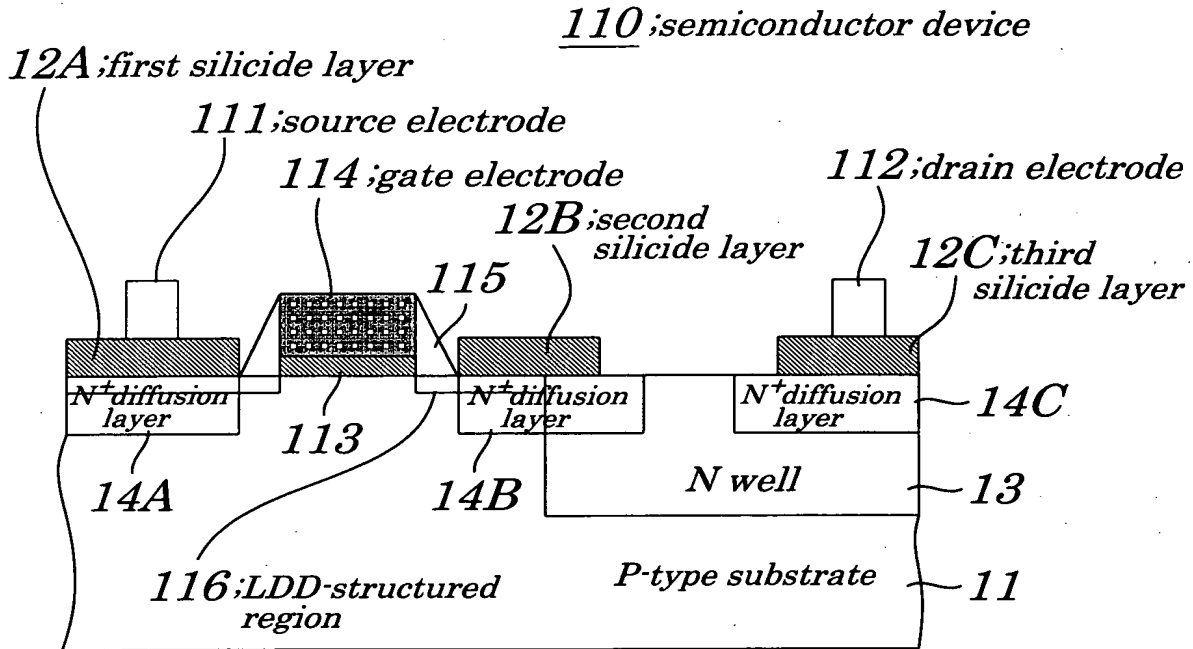
**FIG.15**



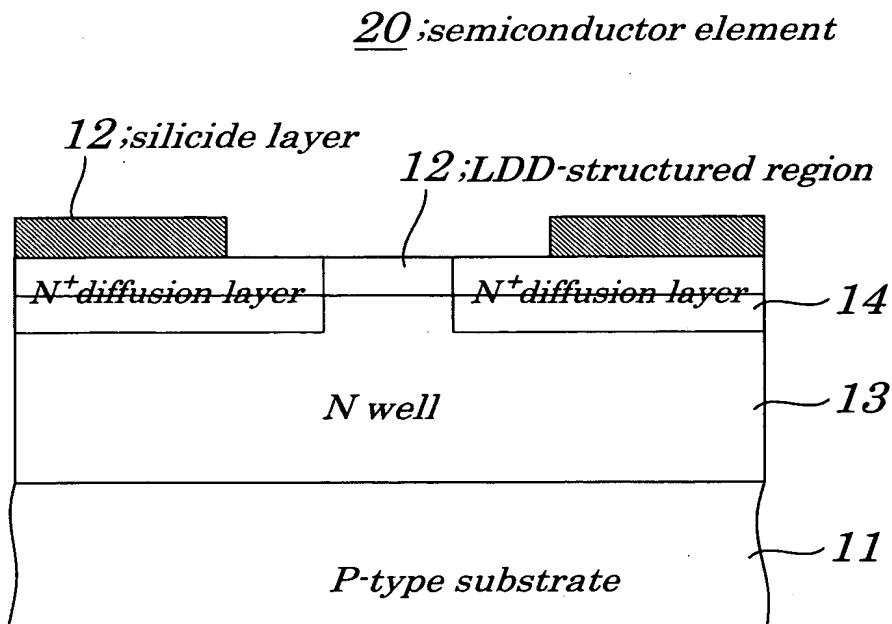
**FIG.16**



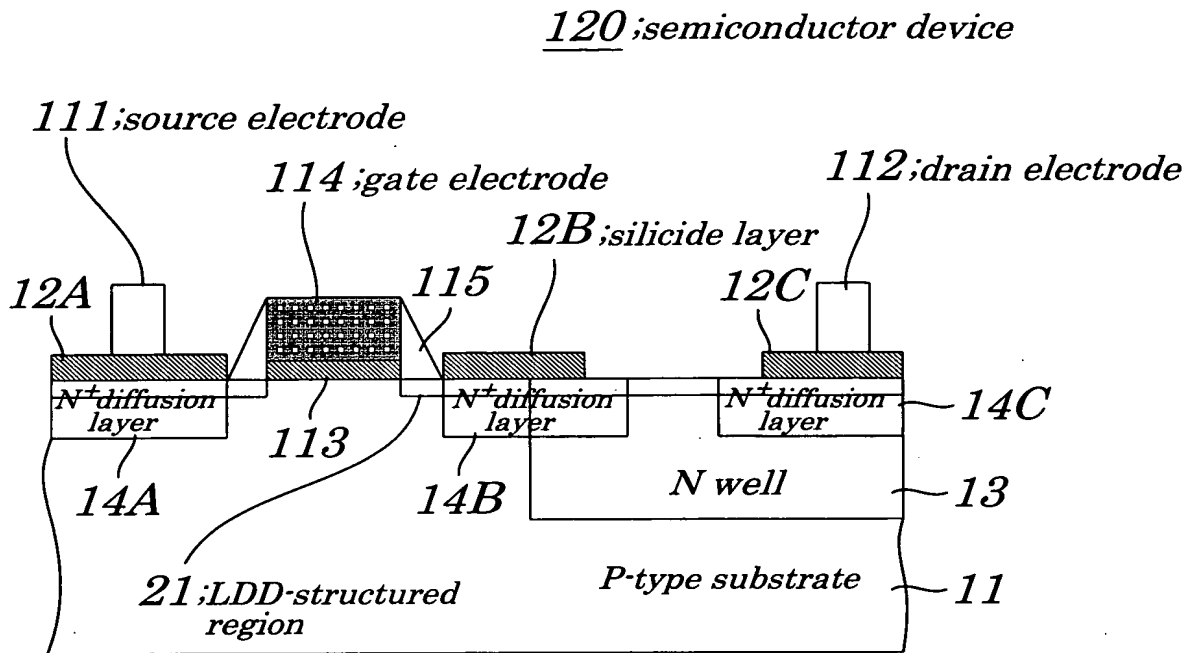
**FIG.17**



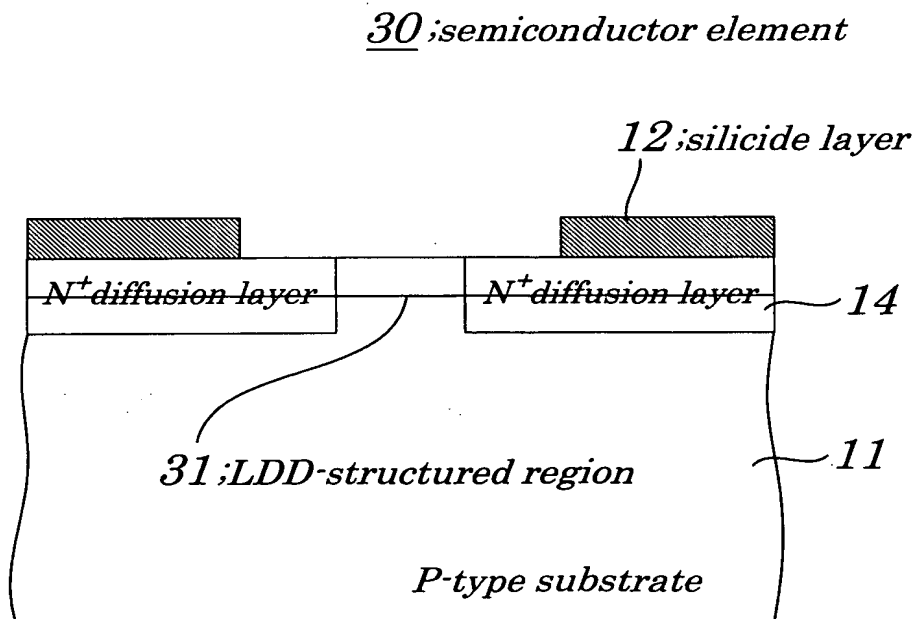
**FIG.18**



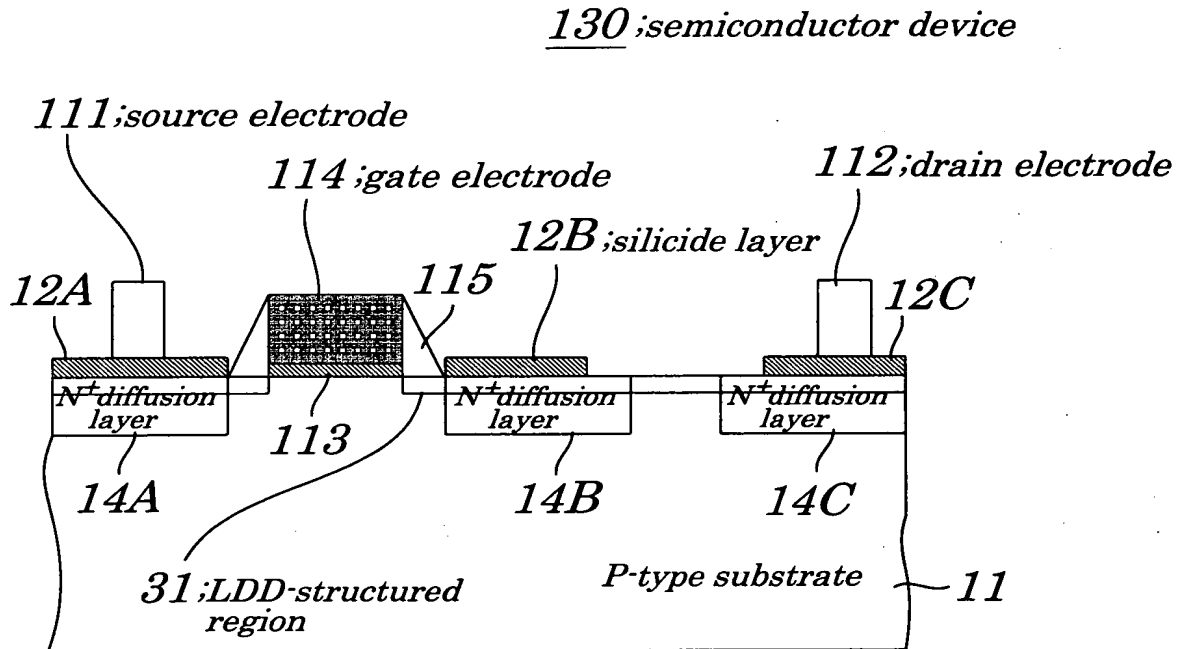
**FIG.19**



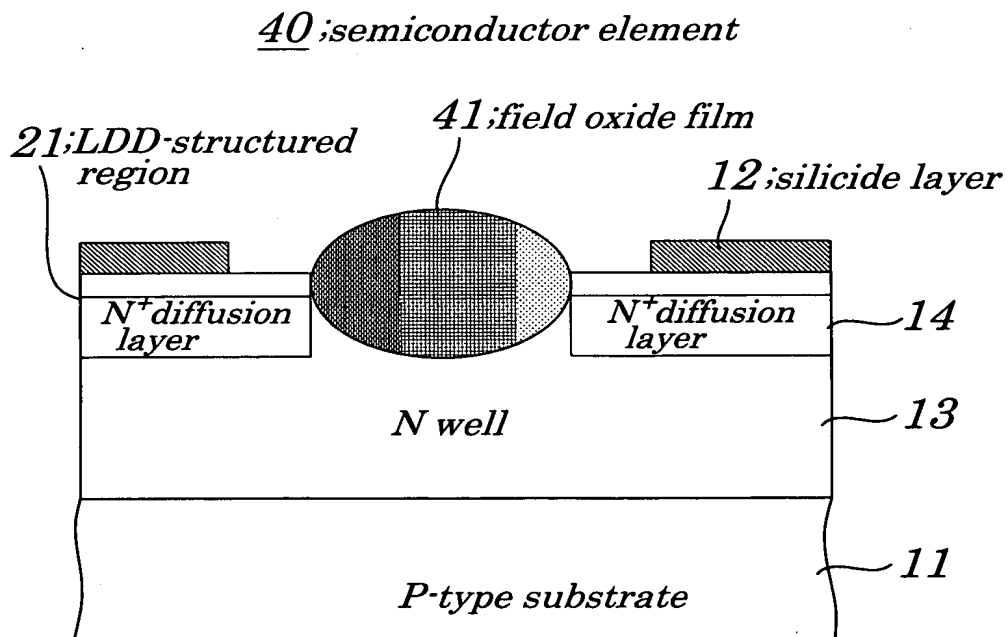
**FIG.20**



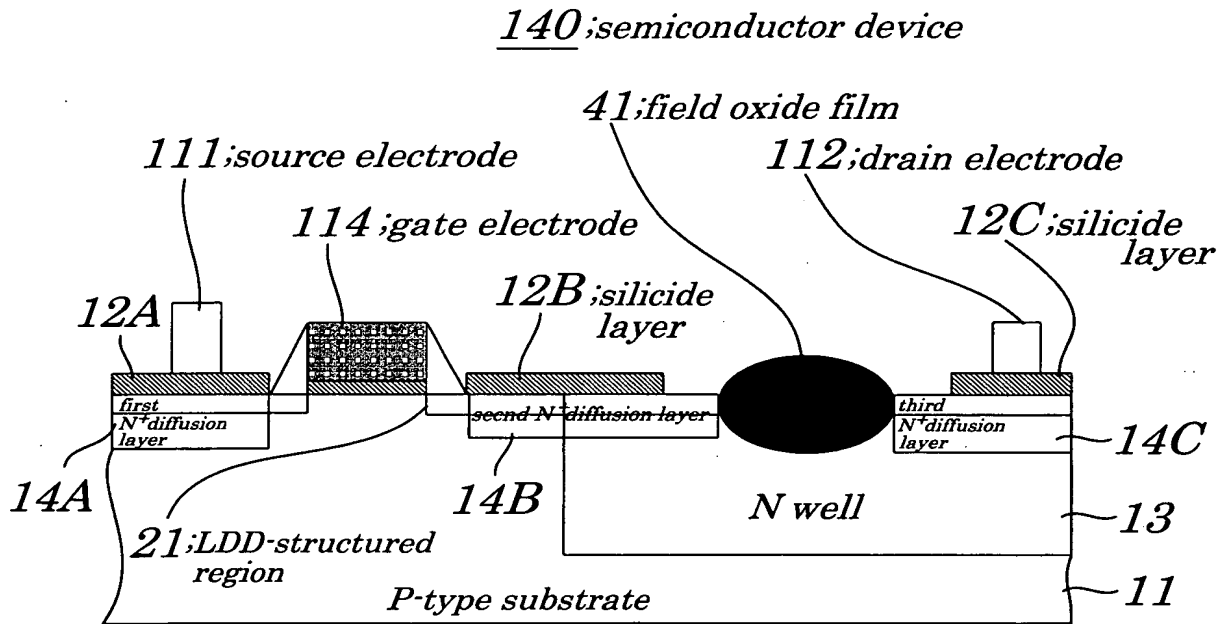
**FIG.21**



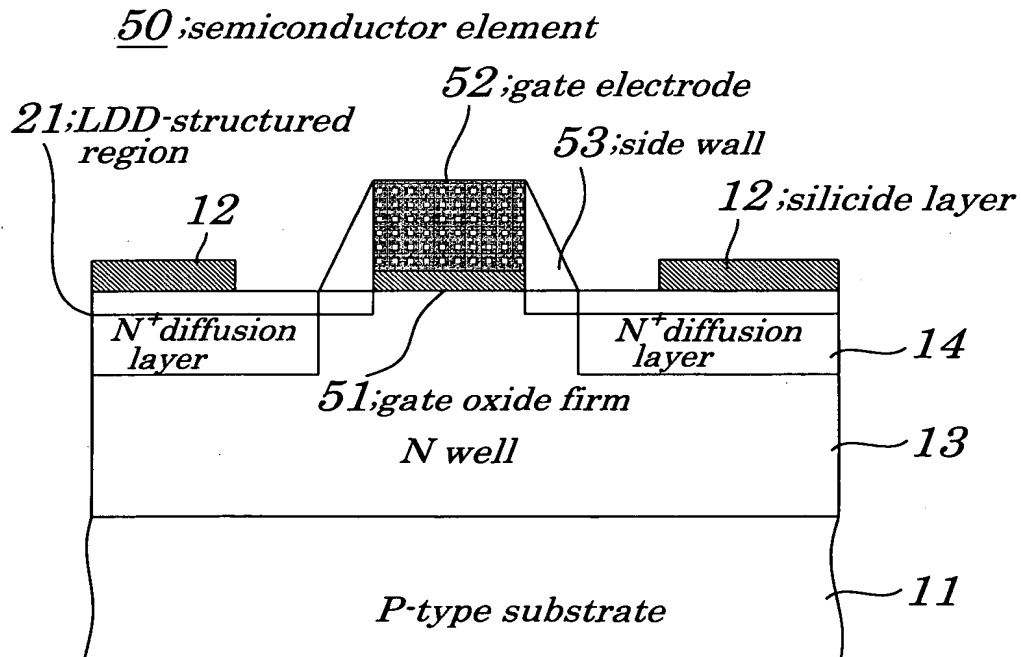
**FIG.22**



**FIG.23**

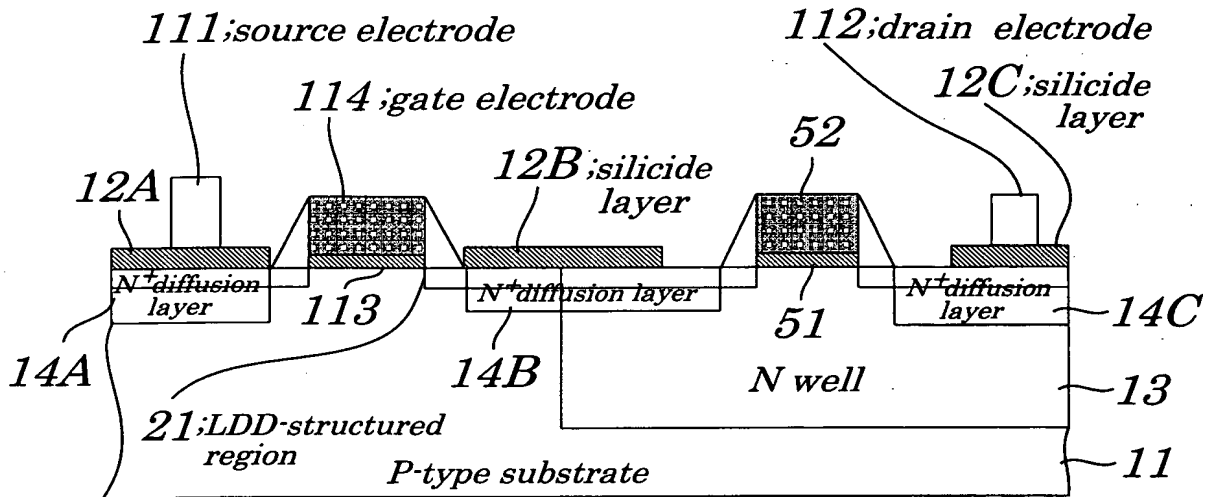


**FIG.24**



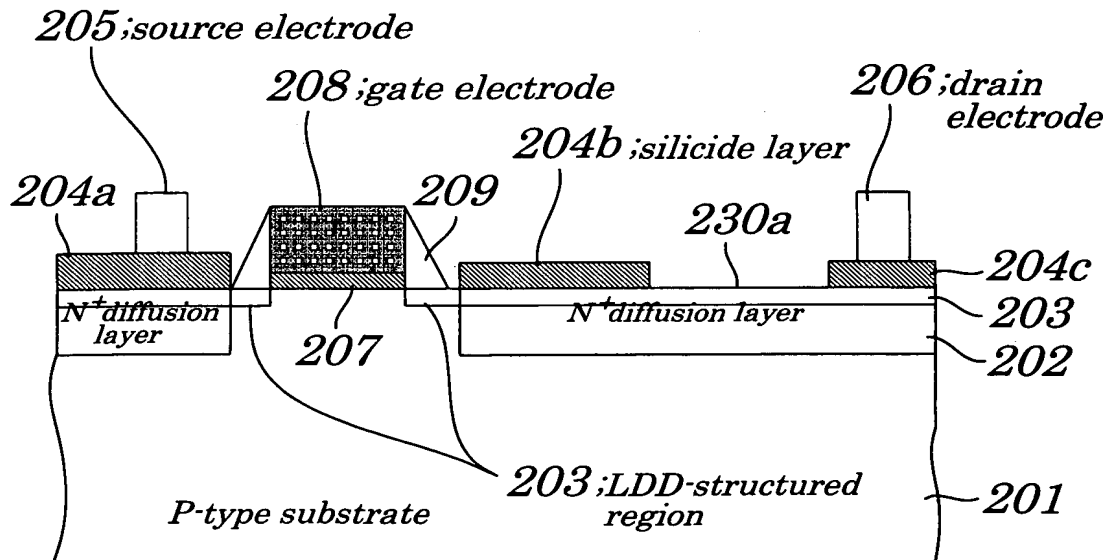
**FIG.25**

150;semiconductor device



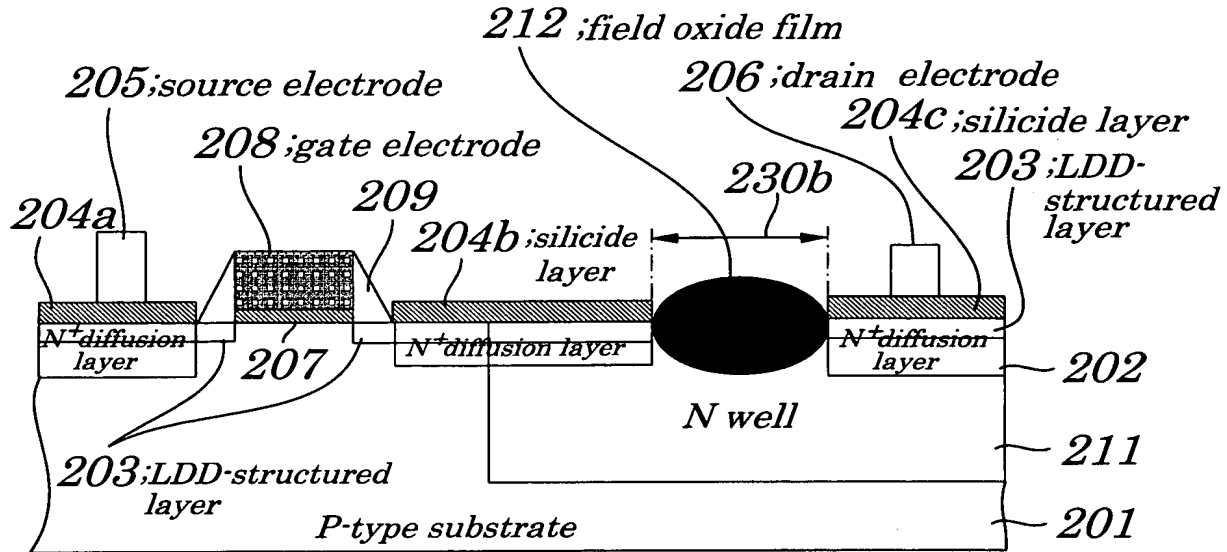
**FIG.26 (PRIOR ART)**

200;semiconductor device



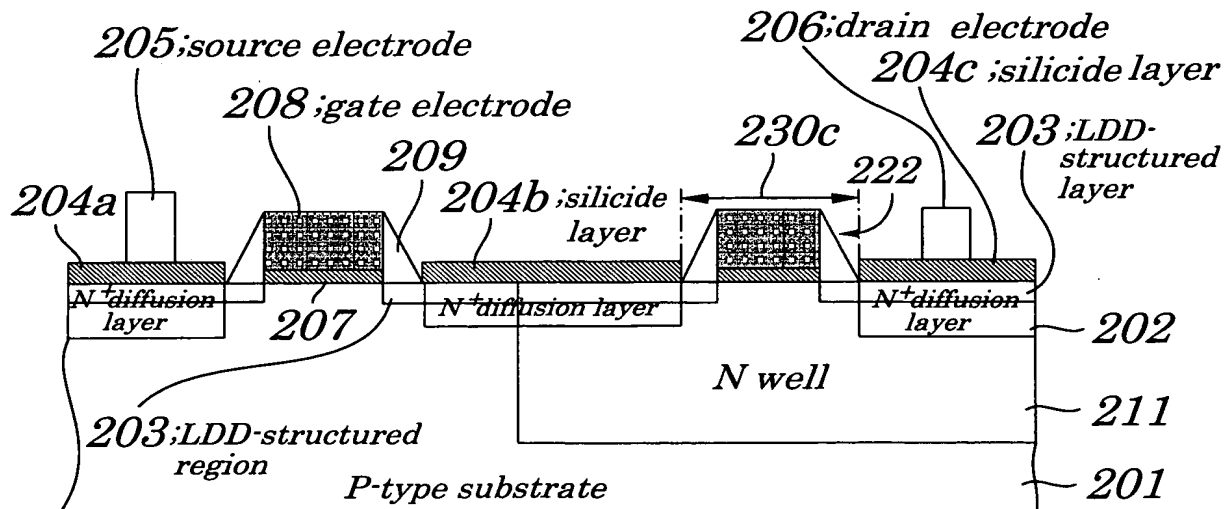
**FIG.27 (PRIOR ART)**

210;semiconductor device



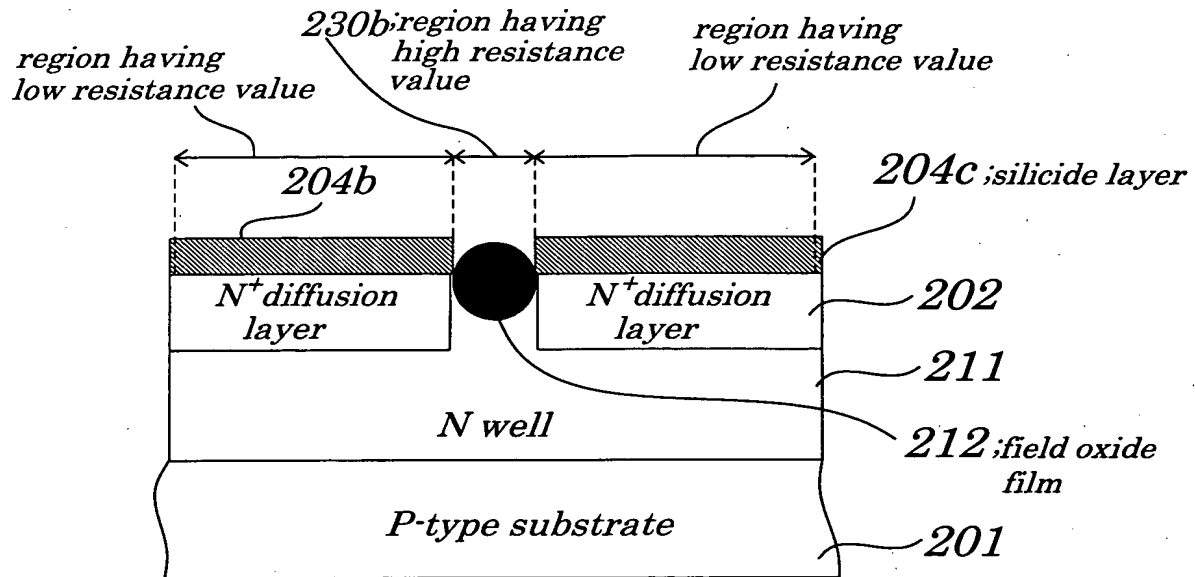
**FIG.28 (PRIOR ART)**

220;semiconductor device





**FIG.29A (PRIOR ART)**



**FIG.29B (PRIOR ART)**

